Hardware Description Language

Course description sheet

Basic information

Field of study Applied Computer Science **Major** - **Organisational unit** Faculty of Physics and Applied Computer Science **Study level** First-cycle (engineer) programme **Form of study** Full-time studies **Profile** General academic	**Didactic cycle** 2020/2021 **Course code** JINSS.li20K.98ced8407ed2037cfd134444a07ed3dd.20 **Lecture languages** polish **Mandatoriness** Obligatory **Block** Core Modules **Course related to scientific research** Yes

Course coordinator	Andrzej Skoczeń
Lecturer	Andrzej Skoczeń

Period Semester 6	**Method of verification of the learning outcomes** Completing the classes **Activities and hours** Lectures: 20 Laboratory classes: 22 Project classes: 15	**Number of ECTS credits** 6

Goals

C1	Provide basic knowledge about the EDA methods of designing equipment for digital systems. To acquaint students with FPGA and ASIC systems.
C2	Presentation of the syntax of the Verilog language and elements of the SystemVerilog language.
C3	Provide knowledge about the basic architectures of digital devices and their modeling in Verilog HDL.
C4	Passing on the ability to create a hardware application using a runtime module with an FPGA chip and a professional design environment.

Course's learning outcomes

Code	Outcomes in terms of	Learning outcomes prescribed to a field of study	Methods of verification
Knowledge – Student knows and understands:			
W1	The student is fluent in the syntax of the Verilog language and is satisfactory in the VHDL language. Understands the importance of the above-mentioned and other hardware description languages in the design flow of digital device.	INS1A_W02, INS1A_W03	Activity during classes, Participation in a discussion, Execution of a project, Test
W2	The student knows and understands the basic concepts discussed in the lecture concerning the analysis and synthesis of combinational and sequential digital circuits. He also knows the basic hardware architectures of control systems and data processing paths.	INS1A_W01, INS1A_W02, INS1A_W05	Activity during classes, Participation in a discussion, Execution of a project, Test
W3	The student has current knowledge of the production technology of very large-scale integrated VLSI digital circuits in two options: ASIC and FPGA (CPLD). He also knows the structure of libraries of standard cells used in the design of digital devices.	INS1A_W01, INS1A_W05	Execution of a project, Execution of laboratory classes
Skills – Student can:			
U1	The student is able to build both a functional and a synthesizable hardware model. He can also carry out a simulation of the constructed model and analyze the obtained results.	INS1A_U04, INS1A_U05	Execution of a project, Execution of laboratory classes
U2	The student is able to create a simple hardware application for control and/or data processing.	INS1A_U05, INS1A_U06	Execution of a project, Execution of laboratory classes
Social competences – Student is ready to:			
K1	The student is able to work in a project team. He can independently acquire the appropriate knowledge and skills necessary to carry out his part of the team task.	INS1A_K01, INS1A_K02	Execution of a project, Project
K2	The student is able to present the completed project in a communicative way. He can also indicate the areas of application of the created applications and the economic aspects of the applied solutions.	INS1A_K01, INS1A_K03	Execution of a project, Project, Report

Program content ensuring the achievement of the learning outcomes prescribed to the module

The course introduces students to the design of digital circuits using FPGA (Field Programmable Gate Array) technology.

Student workload

Activity form	Average amount of hours* needed to complete each activity form
Lectures	20
Laboratory classes	22
Project classes	15
Preparation for classes	10
Realization of independently performed tasks	41
Examination or final test/colloquium	2
Preparation of project, presentation, essay, report	40
Student workload	**Hours** 150
Workload involving teacher	**Hours** 57

* hour means 45 minutes

Program content

No.	Program content	Course's learning outcomes	Activities
1.	Hardware description language as a design tool in microelectronics: Various hardware description and verification languages and areas of their application: HDL: Verilog, SytemVerilog, VHDL, Abel, AHDL. Specificity and comparison with programming languages. Automation of the electronic equipment design process. Current trends in EDA.	W1, W2, W3, U1	Lectures
2.	Microelectronics and programmable circuits: Microelectronics: history and future. Moore's Law. Success of CMOS technology. The concept of mask and technological layers. The current state of development and challenges for CMOS technology. PLD programmable circuit technology. Digital circuit design process.	W1, W2, W3, U1	Lectures

3.	Programmable circuits: PLD structures: ROM, PLA, PAL. Programmable connection technology. Comparison of CPLD and FPGA. The architecture of the Spartan-3x and Zynq-7000 families and other families from Xilinx company. Basic functional blocks, their structure, and their parameters.	W1, W2, W3, U1	Lectures
4.	Chain of algorithms and software tools leading from the model in HDL RTL to the working application in the FPGA system: synthesis, mapping, clustering, layout, routing, bitstream generation.	W1, W2, W3, U1	Lectures
5.	Basics of the Verilog language: language conventions, data types, modules, ports, module instantiation, tasks, functions, compiler directives, gate types. Tasks and system functions.	W1, W2, W3, U1	Lectures
6.	Some of the improvements introduced by the SystemVerilog language: data types, operators.	W1, W2, W3, U1	Lectures
7.	Behavioral modeling in Verilog. Sequential and parallel block, blocking and non-blocking procedural assignment, timing control, conditional instruction, branches, loops. Preparation of the test module.	W1, W2, W3, U1	Lectures
8.	RTL modelling in Verilog language: Data flow modelling: continuous assignments, delays, operators. Simulation models and synthesizable models. Coding style leading to correct synthesis results. Static timing analysis. Timing and physical design constraints.	W1, W2, W3, U1	Lectures
9.	FSM finite automaton: graph and diagram, Moore and Mealy'edgo approach, methods of writing in the Verilog language (SystemVerilog), state coding. Micropramed architecture.	W1, W2, W3, U1	Lectures
10.	Other Verilog constructs: Key-level modeling. Dynamic time analysis. Simulation standard cell library.	W1, W2, W3, U1	Lectures
11.	Behavioural Simulation in Verilog: Learning Outcomes: • the student is able to record the functionality of a digital device in Verilog • the student is able to use the Vivado design environment to a degree that allows the simulation of a model of a simple digital functional block, • the student is able to prepare a testing module in Verilog and interpret the obtained waveforms in a simulation.	W1, W3, U1, U2, K1, K2	Laboratory classes
12.	Verilog RTL code synthesis and post-synthesis simulation: Learning outcomes: • the student is able to write in Verilog a synthesizable model of a digital device, • the student is able to synthesize and simulate the obtained structural model in the Vivado environment.	W1, W3, U1, U2, K1, K2	Laboratory classes

13.	Projecting and commissioning of the SPI bus master module. Educational outcomes: • the student is able to write the synthesized model of the SPI driver according to the given graphs, • the student is able to synthesize and implement this device and observe its work on the hardware.	W1, W3, U1, U2, K1, K2	Laboratory classes
14.	Finite automaton implementation in the Zynq-7000 system: Learning outcomes: • the student is able to create the RTL model of a finite automaton, and carry out its simulation verification, synthesis and implementation in the Zynq-7000 system so that the correctness of the automaton operation can be checked using the knob, buttons, switches, and LEDs available on the training module.	W1, W3, U1, U2, K1, K2	Laboratory classes
15.	Implementation of OLED display driver or UART transmission: Learning outcomes: • the student is able to save the synthesized OLED display driver model (UG-2832HSWEG04 type) according to the given diagrams, • the student is able to save the synthesizable model of the UART transmitter/receiver using IP-Core cooperating with the AXI4-Lite bus, • the student is able to synthesize and implement this device and observe its work on the hardware.	W1, W3, U1, U2, K1, K2	Laboratory classes
16.	Project with the Zynq-7000 system: Students carry out projects in teams of two. Each team is assigned a different randomly assigned project. The starting point for students is the provided assumptions and design guidelines. As part of the project, a working device and documentation of the project should be created based on the hardware resources available in the training module with the Zynq-7000 system. Educational outcomes: • the student is able to interpret the specification of the device in order to build it using the available software tools, • the student is able to effectively use the basic design tools available in the Vivado Xilinx environment to create a simple hardware application on the training module with the Zynq-7000 chip, • the student is able to cooperate in a group by carrying out his part of the task, • the student is able to demonstrate the functionality of the constructed device in accordance with the given specification and prepare documentation.	W1, U1, U2, K1, K2	Project classes

Extended information/Additional elements

Teaching methods and techniques:

E-learning, Lectures, Discussion, Group work, Design thinking, Project based learning, Demonstration, Feedback

Activities	Methods of verification	Credit conditions
Lectures	Activity during classes, Participation in a discussion, Execution of a project, Execution of laboratory classes, Test	lack
Lab. classes	Activity during classes, Participation in a discussion, Execution of a project, Execution of laboratory classes, Test, Project, Report	the presence and results of tests and quizzes
Project classes	Activity during classes, Participation in a discussion, Execution of a project, Execution of laboratory classes, Test, Project, Report	demonstration of a working device, description in the form of a report

Additional info

The course has a website with current information on the UPeL platform.

Conditions and the manner of completing each form of classes, including the rules of making retakes, as well as the conditions for admission to the exam

As part of the computer and electronic laboratory, students work independently (or, in teams of two persons when there are too few setups available) to perform a number of exercises that are treated as necessary preparation for the implementation of the project.
Each meeting in the laboratory begins with a short quiz on the current topic discussed during the lecture. To be credited: at least 30% of the maximum possible number of points must be achieved for each quiz, and the collected points for all quizzes must exceed 50% of the total maximum possible number of points. In the opposite case, the student must complete an additional review quiz. Its score replaces the weakest subscore.
The last meeting in the laboratory part is devoted to a computer practical test consisting of the individual realization of a simple design task:
Each meeting in the laboratory begins with a short quiz on the current topic discussed during the lecture. To be credited:
building a synthesizable model,
simulation,
synthesis and
commissioning on the FPGA system.
The OL score is created from the quizzes and the practical test with 50% weight respectively. This is the first component of the final grade OK.
The design is assessed on the basis of the percentage of the realized design assumptions and the evaluation of the reliability of operation of the created device. The teacher's comments formulated during the assessment require modifications to the project and report. The method of presenting the technical information contained in the developed documentation is also assessed. The OP rating is the second component of the final OK rating.
Passing the computer-electronic laboratory requires passing:

- all the quizzes,
- the practical, computerized test,
- all projects.

The condition for obtaining credit for a single project is:

- successful presentation of the system operation,
- correctly performed measurements,
- successful report/project documentation.,
- successful self-activation by the assessor in the absence of students based on the report.

Method of determining the final grade

The final grade OK in the module is calculated as the normal average of the grade for the cards and practice test OL and the project OP:
OK = 0.5 * OL + 0.5 * OP
OK - final grade
OL - grade from postcards in laboratory classes
OP - project grade

Manner and mode of making up for the backlog caused by a student justified absence from classes

At the end of the semester, there is an additional date for exercises (announced 2 weeks earlier on the website of the course and by the teacher), where you can perform work that the student could not complete on the original date due to random reasons. Students can also make up for any outstanding exercises.

Prerequisites and additional requirements

• Basic knowledge of Boolean algebra
• Basic knowledge of digital electronics
• Basic knowledge of the structure of programming languages
• Knowledge of C syntax is useful

Rules of participation in given classes, indicating whether student presence at the lecture is obligatory

Lecture (optional): Students take part in the classes, learning about the content of the teaching in accordance with the description of the subject. Students should ask questions on an ongoing basis to clarify any doubts and ambiguities that arise. Students should ask questions on an ongoing basis to clarify any doubts and ambiguities that arise. The audiovisual recording of the lecture requires the consent of the lecturer.
Laboratory exercises (obligatory): Students perform laboratory exercises in accordance with the materials provided by the tutor and the presentation conducted by him. The student is obliged to prepare for the subject of the exercise and the information presented during the lecture. Each time it is verified by means of a short written quiz. The student is required to repeat all the presented operations carefully enough to obtain the same functional effect on the exercise module. On this basis, the exercise is passed. Passing the module is possible after passing all laboratory classes.
Design exercises (obligatory): Students perform practical work aimed at acquiring competencies assumed by the description of the subject. The method of project implementation and the final effect are subject to evaluation.

Literature

Obligatory

1. Materiały z wykładu dostępne na stronie przedmiotu w systemie UPeL

Optional

1. B. J. LaMeres, "Introduction to Logic Circuits & Logic Design with Verilog" Springer, 2017
2. Z. Hajduk, "Wprowadzenie do języka Verilog", Wydawnictwo BTC, 2009
3. J. Majewski, P. Zbysiński, "Układy FPGA w przykładach", Wydawnictwo BTC, 2007
4. IEEE Standard Verilog Hardware Description Language, IEEE Std 1364-2001
5. IEEE Standard VHDL Language Reference Manual, IEEE Std 1076-2008
6. IEEE Standard SystemVerilog - Unified Hardware Design, Specification, and Verification Language, IEEE Std 1800-2005

Scientific research and publications

Research

1. Rozwój urządzeń ochrony akceleratora LHC
2. Projekt układu ASIC dla eksperymentu FLAME
3. Transmisja protokołem TRBNET dla eksperymentu PANDA

Publications

1. J.Steckert, A.Skoczeń "Design of FPGA-based radiation tolerant quench detectors for LHC", 2017 JINST 12 T04005
2. P. Hottowy, A. Skoczeń, D.E. Gunning, S. Kachiguine, K. Mathieson, A. Sher , P. Wiącek, A.M. Litke, W. Dąbrowski "Properties and application of a multichannel integrated circuit for low-artifact, patterned electrical stimulation of neural tissue", Journal of Neural Engineering 9 (2012), 066005

Learning outcomes prescribed to a field of study

Code	Content
INS1A_K01	ma świadomość społecznej roli absolwenta uczelni technicznej: zachowującego się profesjonalnie i etycznie, odpowiedzialnego za siebie i zespół, ustawicznie dokształcającego się
INS1A_K02	rozumie pozatechniczne aspekty i społeczne skutki stosowania narzędzi informatycznych
INS1A_K03	rozumie możliwości komeryjnego zastosowania systemów informatycznych
INS1A_U04	potrafi posługiwać się specjalistycznym językiem z zakresu fizyki i informatyki, również w języku angielskim na poziomie B2
INS1A_U05	potrafi wykorzystać uzyskaną wiedzę informatyczną i poznane modele matematyczne do wszechstronnej oceny i diagnostyki systemów informatycznych
INS1A_U06	potrafi dokonać algorytmizacji problemu inżynierskiego i posługując się odpowiednimi metodami i narzędziami potrafi zaprojektować i wykonać odpowiedni system informatyczny
INS1A_W01	zna i rozumie podstawowe zagadnienia z zakresu matematyki i fizyki
INS1A_W02	zna i rozumie zagadnienia z zakresu informatyki i systemów informatycznych
INS1A_W03	zna i rozumie zagadnienia z zakresu struktur danych oraz programowania, w tym w zakresie baz danych i grafiki komputerowej
INS1A_W05	zna i rozumie podstawowe zagadnienia z zakresu elektrotechniki, elektroniki i komputeryzacji pomiarów